VIDEO SWITCHING SYSTEMS AND METHODS

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FIELD OF THE INVENTION

This invention relates generally to video data control and, more specifically, to the control of multiple video data sources between multiple video data outputs.

BACKGROUND OF THE INVENTION

Complex systems having multiple components that provide data for presentation into one of many video data outputs, use complex video switch processors. The video switch processors allow an operator of a system (*e.g.* aircraft) to switch between multiple video sources at a particular display unit. Operator workloads are greatly reduced when they can view data from multiple sources on a single display unit.

Advanced helmets that include video display devices, such as the Strike Helmet 21 program, are most effective if they include connections to multiple video sources, such as multifunction display units included in control panels. Currently available video switches for

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advanced helmets do not have the appropriate quantities of inputs or outputs, do not provide crosspointing (*i.e.*, an input drives one or more outputs simultaneously), are only available in non-rugged or oversized circuit card formfactors, and are controlled by nonstandard communication mechanisms.

Therefore, there exists a unmet need for a video switch for switching between multiple inputs and multiple outputs in an easy to implement form.

SUMMARY OF THE INVENTION

The present invention is directed to systems and methods for performing video switching between multiple inputs and outputs. In one embodiment, a system includes a video box coupled to one or more user interfaces, a plurality of video inputs, and a plurality of video outputs. The video box includes a video controller coupled to the one or more user interfaces and a video switch coupled to the plurality of video inputs and the plurality of video outputs. Activation of one of the user interfaces generates a video control signal that is sent to the video controller. The video controller generates a video switching signal based on the received video control signal. The video switch connects one or more of the plurality of video inputs to one or more of the plurality of video outputs based on the generated video control signal.

In accordance with further aspects of the invention, the plurality of video inputs include 16 video inputs and the plurality of video outputs include 16 video outputs.

In accordance with other aspects of the invention, one or more of the plurality of video outputs include a helmet display device.

In accordance with another aspect of the invention, the video box includes a Peripheral Component Interface (PCI) data bus for delivering the video switching signal.

In accordance with still further aspects of the invention, the video switch includes an interface device coupled to the data bus and a switch coupled to the interface device and the plurality of video inputs and outputs. The video switching signal is received by the interface device over the data bus. The interface device generates a video switch instruction based on the received video switching signal and sends the generated video switch instruction to the

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switch. The switch connects one or more of the video inputs to one or more of the video outputs according to the video switch instruction.

In accordance with still another aspect of the invention, the video switch is implemented on a circuit card that is formed according to the PCI mezzanine card (PMC) formfactor. The circuit card is a high temperature and conduction cooled card for use in a commercial-off-the-shelf (COTS) avionics box. The PMC formfactor allows the switch to be installed on an existing full-size circuit card, such as a VME card in the case of the advanced helmet Electronics Unit (EU), and to be controlled by the PCI data bus native to the VME card.

BRIEF DESCRIPTION OF THE DRAWINGS

The preferred and alternative embodiments of the present invention are described in detail below with reference to the following drawings.

FIGURE 1 is a block diagram of an embodiment of a system formed in accordance with the present invention;

FIGURE 2 is a block diagram of an embodiment of a switch device formed in accordance with the present invention; and

FIGURE 3 is a block diagram of an embodiment of control logic within a switch device in accordance with a further embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is directed to systems and methods for providing crosspoint switching between multiple video inputs and multiple video outputs. Many specific details of certain embodiments of the invention are set forth in the following description and in FIGURES 1–3 to provide a thorough understanding of such embodiments. One skilled in the art, however, will understand that the present invention may have additional embodiments, or that the present invention may be practiced without several of the details described in the following description.

As shown in FIGURE 1, in one embodiment, a video controlling system 20 includes a video box 24 and a user interface 26. The video box 24 includes a video controller 30 coupled via a data bus to a video switch 32. The video switch 32 is coupled to a plurality of

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video inputs (*e.g.*, a weapons system, flight data computer, etc.) and a plurality of video outputs (*e.g.*, flight data recorder, helmet mounted displays, etc.). The user interface 26 is controlled by an operator, such as without limitation a pilot, for generating a video selection signal. The video selection signal is sent to the video controller 30 that sends a video switching signal to the video switch 32. Based on the switch signal, the video switch 32 makes a connection between one or more of the video inputs and one or more of the video outputs. The video switch 32 is described in more detail below with reference to FIGURES 2 and 3.

In one embodiment, as shown in FIGURE 2, the video switch 32 includes an interface chip 60, control logic 62, and a video crosspoint switch 64. The interface chip 60 is coupled to an external data bus and to the control logic 62 via an internal (local) data bus. The control logic 62 is coupled to the video crosspoint switch 64 which, in turn, is connected to input and output video sources via a pin connection 68. In a preferred embodiment, the video switch 64 may route up to sixteen analog composite video sources in one of a number of different video formats (*e.g.* RS-170, National Television System Committee (NTSC), Phase Alternation Line (PAL), RS-343, etc.) to up to sixteen video destinations.

The components of the video switch 32 may be implemented on a circuit board designed according to the Peripheral Component Interconnect (PCI) Mezzanine Card (PMC) formfactor, defined by the IEEE 1386.1 specification, as well as a conduction-cooled variant defined by ANSI/VITA-20.

In one particular embodiment, the interface chip 60 is a PCI interface chip that is connected to a PCI data bus via PMC connectors PN1 and PN2. Connectors PN1 and PN2 are both 64 pin connectors. The specifications for PMC allow for up to four 64 pin connectors; PN1 and PN2, for carrying power and the basic PCI interface. PN3 is an optional connector to provide 64bit data bus as opposed to the 32bit bus provided by PN1 & PN2. PN4 is an optional, device defined 64 pin connector, that is being used for our video signals.

Switch control commands are sent to the video switch 32 on the PCI bus, which are then placed on the local bus of the video switch 32 by the PCI interface chip 60 for collection and interpretation by control logic 62. The control logic 62 sends signals to the switch 64 for

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setting appropriate registers in the video crosspoint switch 64 to control the routing of video inputs to video outputs.

In another embodiment, the interface chip 60 is preferably a PLXTech PCI9030-AA60PI chip, which supports a 32 bit/33 MHz PCI bus. The PCI9030 chip may respond to PCI read and write commands received from the video controller 60 or may selfinitiate PCI transactions. The PCI9030 chip may use three of six available Base Address Registers (BARs) to map into the PCI bus. The first two BARs may be used to map PCI9030 configuration registers into PCI memory and I/O space respectively, while the third BAR maps a single 32-bit word from the local bus of the video switch 32 into PCI memory space. The video controller 30 may send (*i.e.*, write to appropriate location on the PCI bus) 32-bit command words to the video switch 32 to control the video switch 32. When a command word is written to the appropriate location on the PCI bus, the PCI9030 chip writes the command word to the local bus for retrieval by the control logic 62. Because there is only a single memory location accessible by the video controller 30, all command words are written to the same location, and the control logic 62 is responsible for buffering and handling multiple command words written in succession.

The command word includes information to set the state of a single output on the crosspoint switch 64. In one embodiment, the word is partitioned as follows:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	O3	O2	O1	O0	OE	I3	I2	I1	I0

Bits 8-5 of the command word form the video output selection field O3-O0, which selects which of the sixteen video outputs 0–15 this command word will configure. Bit 4 is an Output Enable flag, which if set to 0 configures the output indicated by the output selection field to a high impedance, (*i.e.*, undriven state). If the Output Enable flag is set to 1, then the output indicated by the output selection field is driven by the signal at the input designated by an input selection field I3-I0 in bits 3-0. Bits 31-9 are reserved and are set at zero. It will be appreciated that the structure of the command word can be altered provided all communicating components understand what the structure is.

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To change more than one output routing the host device must simply write multiple 32-bit command words to this PCI location. This is done to simplify the control logic instead of parsing multiple switch configurations in a single command word. This can be accomplished, because the speed of the interface bus is dramatically faster than the "data rate" of video; all 16 video outputs can be commanded to switch sequentially in less time it takes to draw a single line of video on a screen.

The following is an example C language driver generated by the video controller 30 for configuring the video switch 32:

```
typedef struct
{
    unsigned char inchan;
    unsigned char enabled;
} ChanVal;

typedef struct
{
    int b;
    int d;
    int f;
    unsigned long *address;
    ChanVal outchan [16];
} SwitchHandleStruct;

static SwitchHandleStruct shs;

SwitchHandle
SwitchInit ()
{
    int i;
    unsigned long sendval = 0;

    memset (&shs, 0, sizeof (SwitchHandleStruct));

    if (pciFindDevice(0xBAAC, 0x0001, 0, &shs.b, &shs.d, &shs.f) == ERROR)
    {
        return 0;
    }

    pciConfigInLong(shs.b, shs.d, shs.f, PCI_CFG_BASE_ADDRESS_2, (int
*) (&shs.address));
```


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```
    for(i=0; i < 16; i++)
    {
        sysOutLongNoSwap((int)shs.address, sendval);
        shs.outchan[i].inchan = (unsigned char)i;
        shs.outchan[i].enabled = 0;
        sendval += 0x21; /*Increments 0-3 and 5-8*/
    }

    return 0;
}

int
SetSwitch(SwitchHandle sh, unsigned char outchan, unsigned char inchan,
Unsigned char enabled)
{
    unsigned long sendval = 0;

    shs.outchan[outchan].inchan = inchan;
    shs.outchan[outchan].enabled = enabled;

    sendval = (outchan & 0xf) << 5;
    if(enabled)
      sendval |= 0x10;
    sendval |= (inchan & 0xf);
    sysOutLongNoSwap((int)shs.address, sendval);

    return 0;
}

int
GetSwitch(SwitchHandle sh, unsigned char outchan, unsigned char* inchan,
Unsigned char *enabled)
{
    *inchan = shs.outchan[outchan].inchan;
    *enabled = shs.outchan[outchan].enabled;

    return 0;
}
```

In yet another embodiment, the control logic 62 may be a Field Programmable Gate Array (FPGA), such as an Altera Flex 10K40 FPGA model EPF10K40RC208-3, that has been programmed to configure the FPGA to implement the control logic shown in FIGURE 3. The FPGA reads command words placed on the local bus by the interface

chip 60. As shown in FIGURE 3, an FPGA 100 includes local bus control logic 110 coupled to a command word first in first out (FIFO) buffer 112, which is coupled to a Switch Control state machine 116. The local bus control logic 110 interprets local bus control signals, such as Write Enable (WR_n), Address Select (ADS_n), Wait and Ready states (Wait_n), and Local Write Enable (LWR_n), received from the interface chip 60 to interface the incoming command word with the 32-bit wide by 24-word deep FIFO 112. The FIFO 112 may buffer multiple successive command words, because in one representative embodiment, the PCI bus may be a 33MHz bus while the interface to the crosspoint switch chip may operate at 750kHz. If more command words are sent than there is room in the FIFO 112, the local bus control logic 110 may halt the PCI data bus transaction until the FPGA 100 can catch up, effectively forcing the video controller 30 to wait.

With continued reference to FIGURE 3, the Switch Control state machine 116 checks the command word FIFO 110 for waiting command words, retrieves the oldest command word, and breaks the command word into the components the crosspoint switch chip expects. With the input select values (Insel), output select values (Outsel), and output enable flag value (OE flag) driven to the crosspoint switch, the Switch Control state machine 116 latches the input and output command values into the crosspoint switch. CE_n is chip enable. CE_n is asserted on the crosspoint switch chip before the video crosspoint switch 64 will accept any interface changes. Since the crosspoint switch 64 is the only device on this particular bus except for the FPGA 100, the crosspoint switch 64 can be asserted continuously. After the values have been latched, the Switch Control state machine 116 strobes an update signal (Update_n) to the crosspoint switch, thereby, changing the routing within the crosspoint switch.

In one embodiment, the video crosspoint switch 64 is an Analog Devices AD8115AST chip. The video crosspoint switch 64 routes inputted video signals to video outputs. The video crosspoint switch 64 may amplify a single video input signal that is to be propagated to multiple video outputs. In the above-referenced preferred embodiment, the sixteen video signal inputs coupled to the crosspoint switch 64 include a pair of wires each, one for the signal and one for a return. All analog video signals require a return wire for current return, ground reference, and impedance matching. This is the outer conductor on

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coaxial video wire. The sixteen output signals also are paired, for a grand total of 64 wires to be routed off of the video switch 32. With regards to PMC specifications, the 64 pin PN4 connector connects to the 64 wires.

The video switch 32 may be installed on a host device (not shown) such as a single board computer (SBC) that may include a variety of formfactors. The host device may provide electrical power to the video switch 32. In one embodiment, power on the SBC comes in four voltages, +5VDC, +3.3VDC, +12VDC, and –12VDC, and is provided on connectors PN1 and PN2 according to the PMC specification. The host device provides a PCI bus for the video switch 32 to attach to. The PCI bus may be implemented on connectors PN1 and PN2 according to the PMC specification. The video switch 32 relies on a PCI data bus master on the host device, usually a CPU chip (*i.e.*, video controller 30) such as a Motorola PowerPC or an Intel Pentium, for commands. The host device routes signals from a connector PN4 to points where video sources and destinations can be connected.

In one embodiment, the video switch 32 is designed to operate in a high temperature, low airflow condition. In one exemplary embodiment, for example, the operational temperature range is –25°C to 71°C, measured at thermal interfaces included on the video switch 32. The video switch 32 may conform to the Conduction Cooled PMC specification ANSI/VITA-20, which requires the host device to sink heat away at the thermal interfaces, usually with metal rib mounting points. The video switch 32 may operate in traditional airflow cooled environments with hosts that conform to IEEE 1386.1.

While the preferred embodiment of the invention has been illustrated and described, as noted above, many changes can be made without departing from the spirit and scope of the invention. Accordingly, the scope of the invention is not limited by the disclosure of the preferred embodiment. Instead, the invention should be determined entirely by reference to the claims that follow.

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